Troubleshooting Clock Jitter and Identifying PDN Sensitivities

Quickly identify PDN sensitivities, in-circuit, including clock jitter source locations, using a simple probe-based solution

Power distribution network ('PDN') noise is one of the most common issues in low power applications. Whether you are powering ADCs, clocks, LNAs, digital data networks or sensitive RF applications, properly tuning your power supply is of the utmost importance. These sensitive circuits can be disrupted by just a few millivolts of power supply noise or even less. Due to this extreme sensitivity and the interaction between the power supply, distribution network and load, power supply troubleshooting often becomes necessary.

Due to the interactions between the source and load impedance, the troubleshooting must be performed in-circuit and there is often very limited physical access. As a result, this can be a time consuming process.

Even in a circuit that appears to be fully functional it's generally a good idea to evaluate power supply sensitivities. It's the best way to identify potential issues that could crop up as a result of operational and environmental tolerances.

In this sample application, we will demonstrate some simple test tools, that couple with your spectrum and network analyzers, that help support power supply noise source investigation. Figure 1 shows the Picotest VRTS3 training demo board, which includes a variety of sample circuits, supporting many types of measurements. One of these sample circuits is a 125MHz clock (OSC401), powered by a low dropout (LDO) voltage regulator (U301). Four different output capacitors can be connected or disconnected from the LDO using a four position dipswitch (S301), altering the stability of the power supply.

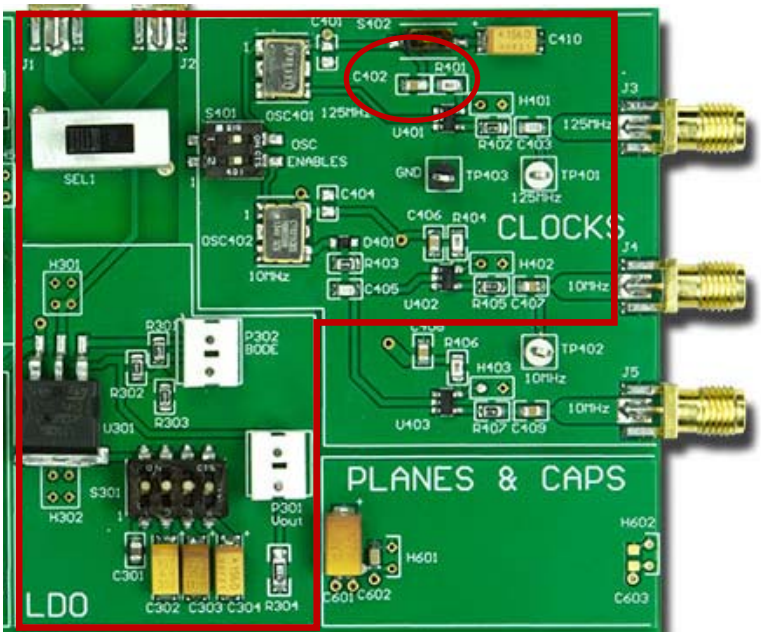


Figure 1: The Picotest VRTS3 training demo board showing the LDO and clock layout.

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The circuit schematic in Figure 2 shows the LDO linear regulator (LT1086) that powers the 125MHz clock oscillator, OSC401 through a slide switch (SEL1). Of note is the 0.01uF decoupling capacitor C402 (on the right).

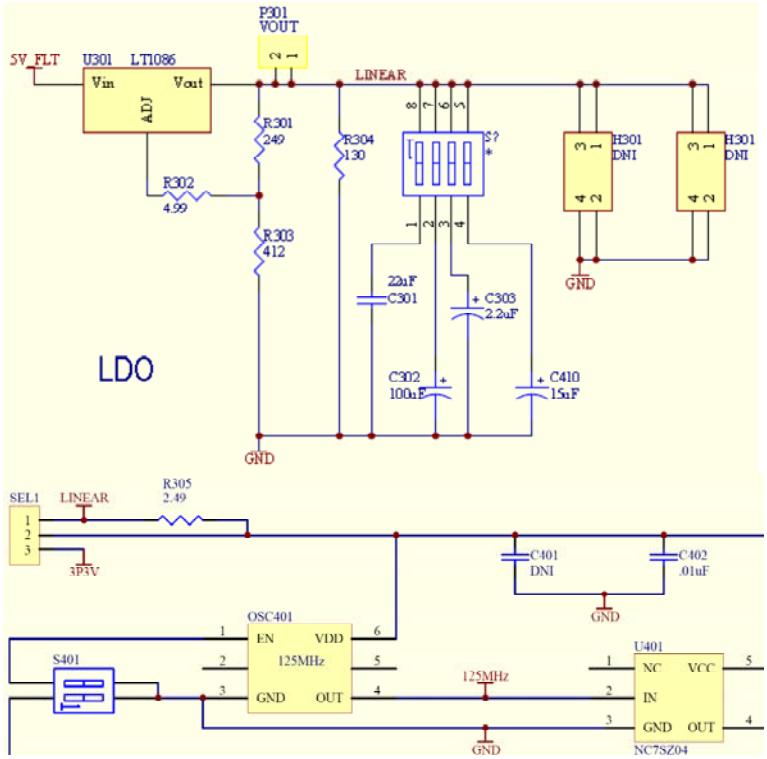


Figure 2: The LDO and clock circuitry schematic.

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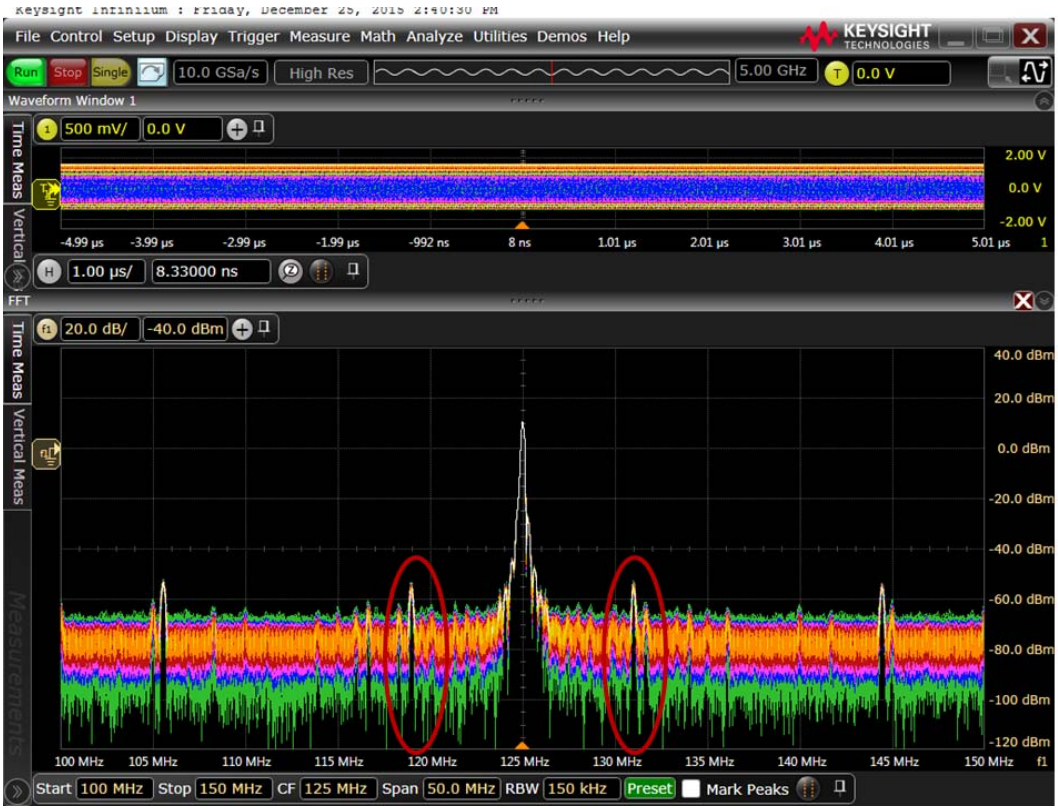


Figure 3: Clock spurs at approximately 6 MHz offset are highlighted in this oscilloscope spectrum plot. These spurs are used to demonstrate a simple and fast troubleshooting technique.

Identifying a power supply noise sensitivity can be accomplished quickly and easily using a wide band harmonic comb generator and a 1-port passive transmission line probe.

The J2150A harmonic comb provides a wideband noise source with a 50Ω output impedance. It is contained in an ultra-portable USB “stick” form factor. The harmonic comb provides noise over a frequency range of 1kHz to more than 1GHz in three frequency ranges. The ranges are centered around 1kHz, 100kHz, and 8MHz. Harmonics are generated by time and frequency dithering of the output impulses. The comb can step through these ranges automatically or be locked onto a single frequency range. While most instruments have several unused USB ports available, the comb can also be powered from the popular cell phone backup batteries for a portable solution.

A wideband DC block is generally included between the comb injector and the probe in order isolate the 50Ω DC impedance from circuit being tested. The clock spectrum is viewed on an oscilloscope with a spectrum analyzer option, a Signal Source Analyzer or a Spectrum Analyzer. The voltage regulator stability and distribution impedance are easily seen as sidebands or jitter in the clock spectrum.

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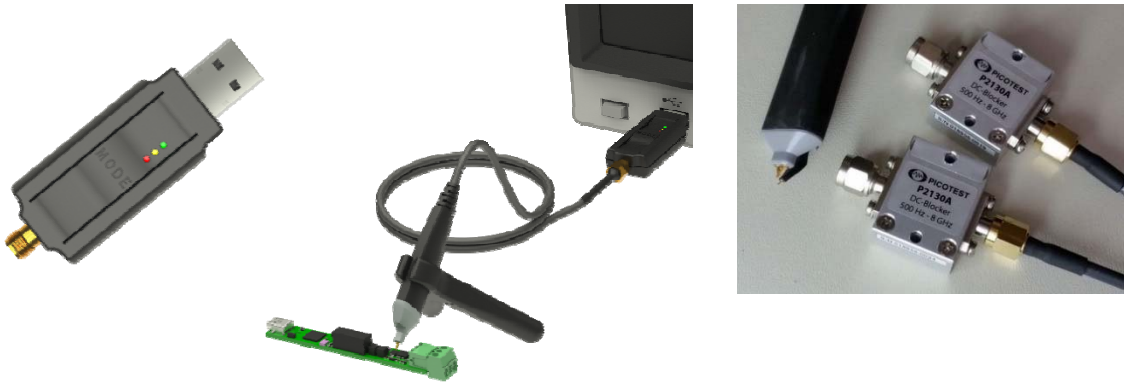


Figure 4: Simple but effective tools support PDN interrogation and clock jitter assessment. These include a J2150A harmonic comb broadband signal generator (left) along with 1-Port (center) and 2-Port bi-directional 50 Ω passive probes and DC blockers (left).

The Picotest transmission line probes are unique, providing unity gain, bidirectional 50Ω connections to various instruments with a comfortable browser style head for probing the power distribution network. This allows the probe to be used to inject signals, as in this example, or to measure noise using the same probe. The probe connection is a generic 50Ω SMA connector, allowing connection to most instruments.

In this example, the harmonic comb injects a broadband signal into the clock's decoupling cap (C402) using the 1-Port Probe, as seen in Figure 4. The clock's spectrum is monitored at SMA connector, J3.

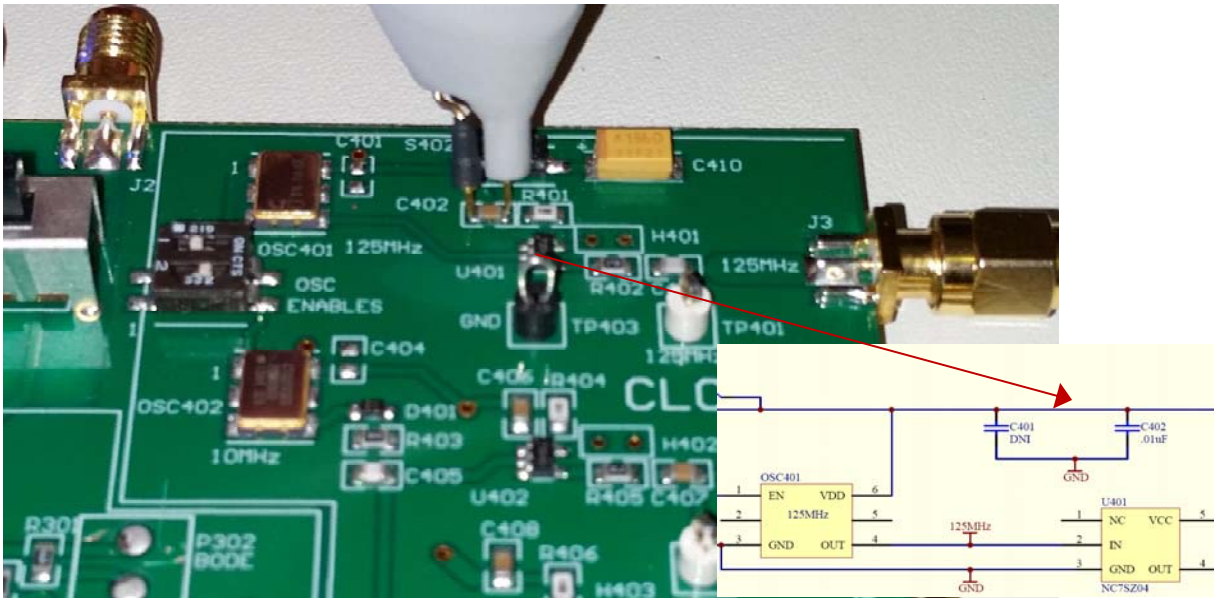


Figure 5: The J2150A harmonic comb (inset and in Figure 3) is connected to the 1-Port probe via a P2130A DC Blocker and used to inject a signal into C402 (VDD of a 125MHz clock oscillator). The clock spectrum is monitored at SMA connector, J3.

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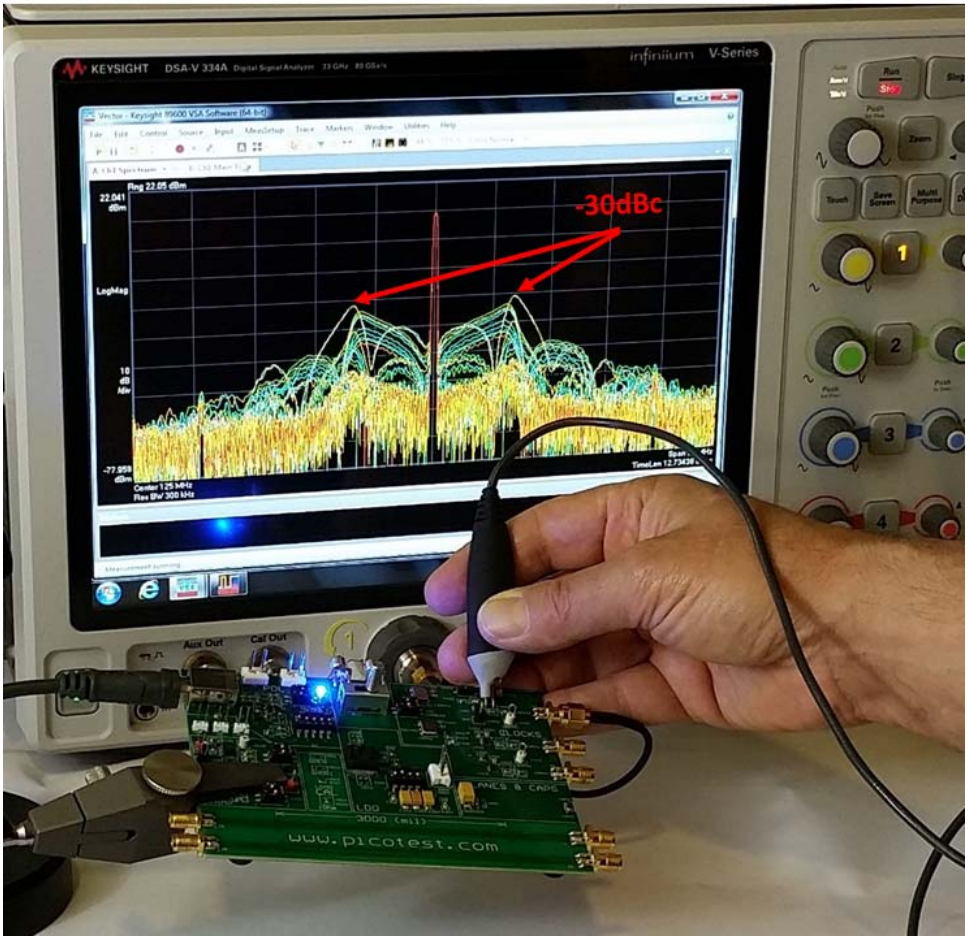


Figure 6: The PDN interrogation using the comb's search mode signal set reveals a resonance at approximately 7.5MHz as seen in the spectrum sidebands around the clock fundamental frequency. Note the peaks are approximately -30dBc.

Moving the noise injection point to the linear regulator (same printed circuit board trace but downstream of the clock) we notice that the clock sideband noise is much smaller in Figure 7 at -45dBc. This information tells us that resonance is between the regulator and the clock.

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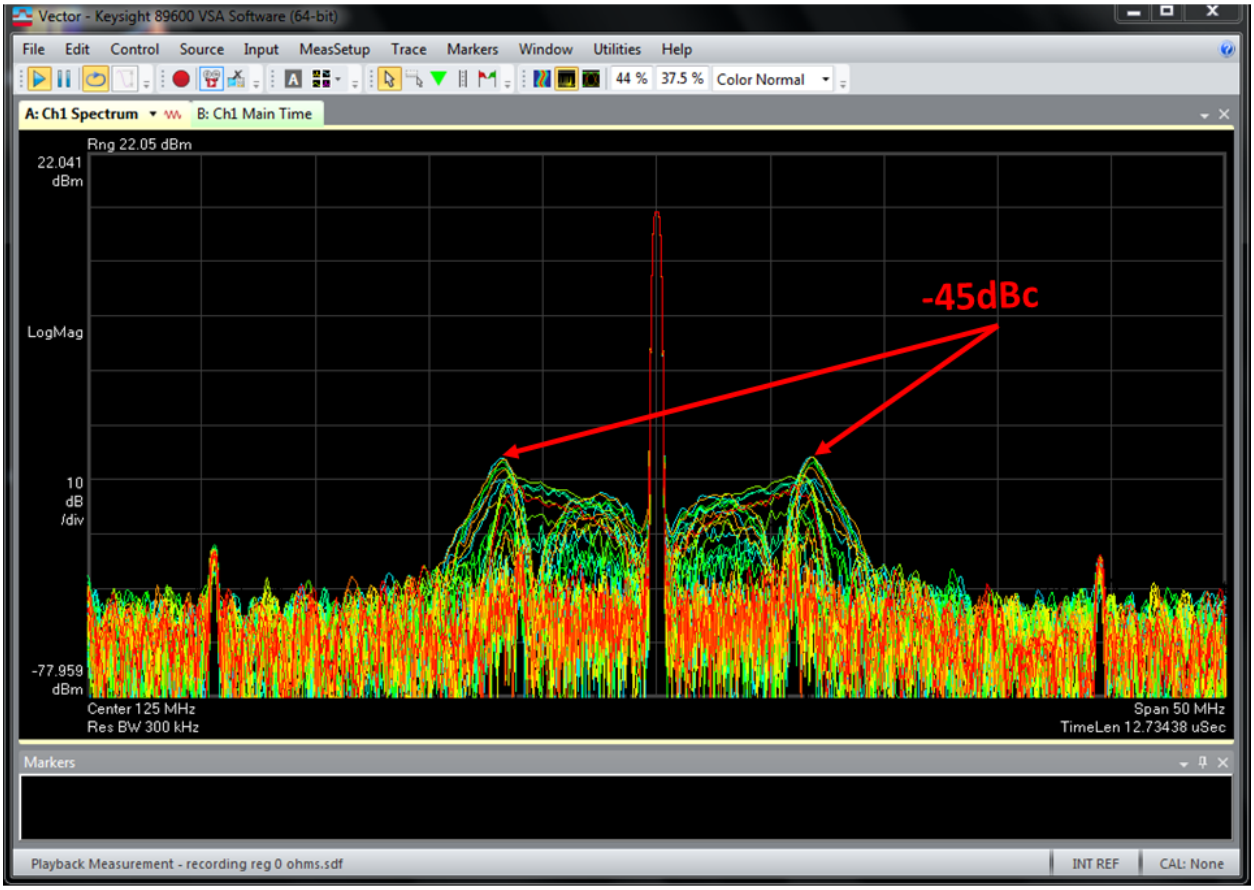


Figure 7: By injecting the noise at different locations within the PDN, the noise source is quickly located. Note the sidebands are about 15dB lower than in Figure 6. This tells us that the resonance is at the clock and not at the regulator.

Having located the resonance at the clock, we can calculate the characteristic impedance of the PCB connection using the value of the decoupling capacitor (10nF) and the 7.5MHz resonant frequency (7.5MHz). The characteristic impedance can be calculated as 1/(2*PI*7.5MHz*10nF), in this case 2.1Ω. Placing SEL1 switch in the center (OFF) position inserts a 2.4Ω resistor (R305) between the linear regulator and the clock, damping the resonance. The elimination of the 7MHz clock spectrum sidebands, seen in Figure 8 confirms that the resonance has been effectively damped by increasing the series resistance between the linear regulator and the clock.

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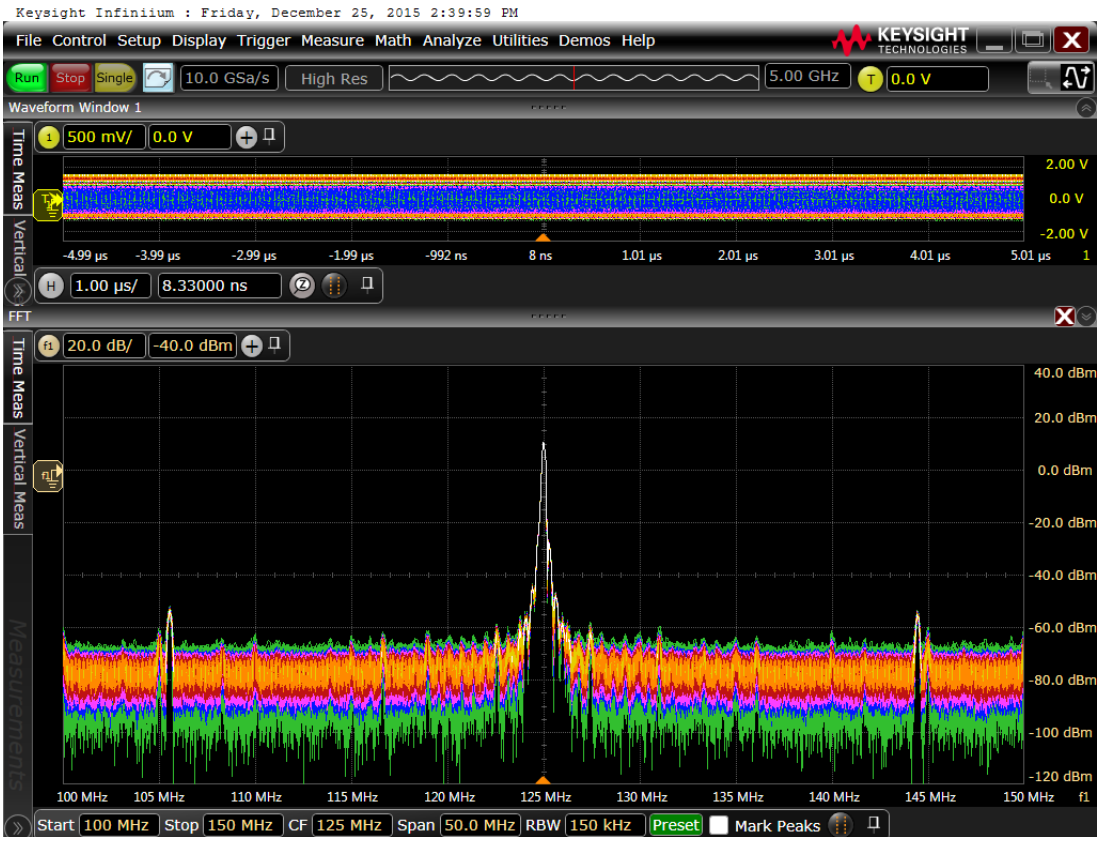


Figure 8: The 7MHz clock sidebands have been eliminated by inserting the series resistor between the regulator and the clock, damping the PCB resonance.

The resonance and the damping effectiveness can easily be confirmed by measuring the impedance at the clock's decoupling capacitor with a vector network analyzer (VNA). Measurements are shown in Figure 10 for two different linear regulator output capacitors, as well as, the insertion of R305.

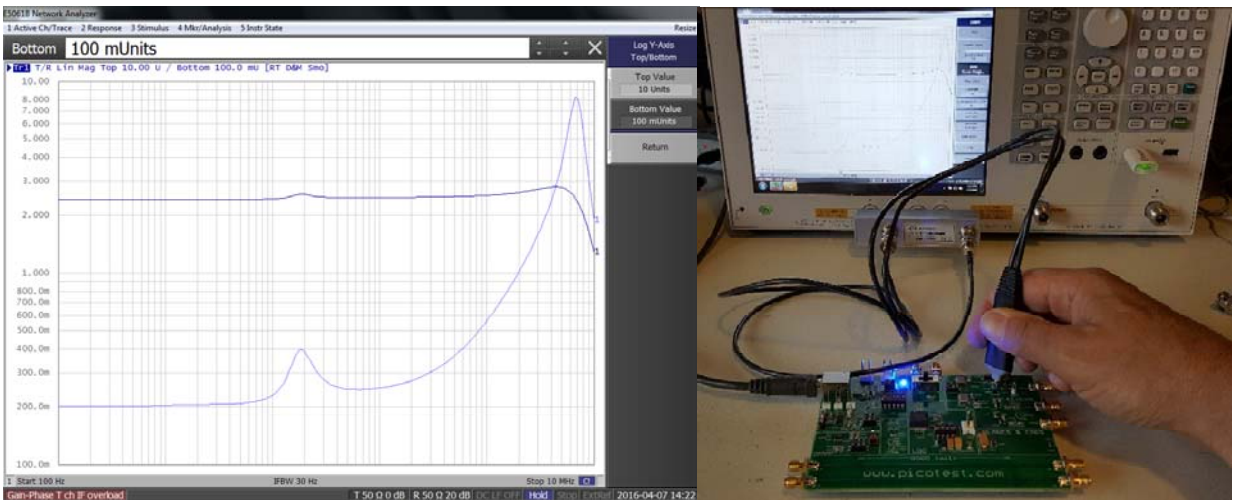


Figure 9: The 7.5MHz resonance (trace with peaking) is clearly seen by measuring the linear regulator output capacitors using the Picotest P2101A 2-Port probe and J2160A adapter. The insertion of the

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2.4Ω resistor damps the resonance (flat trace), reducing the impedance at 7.5MHz by approximately 15dB.

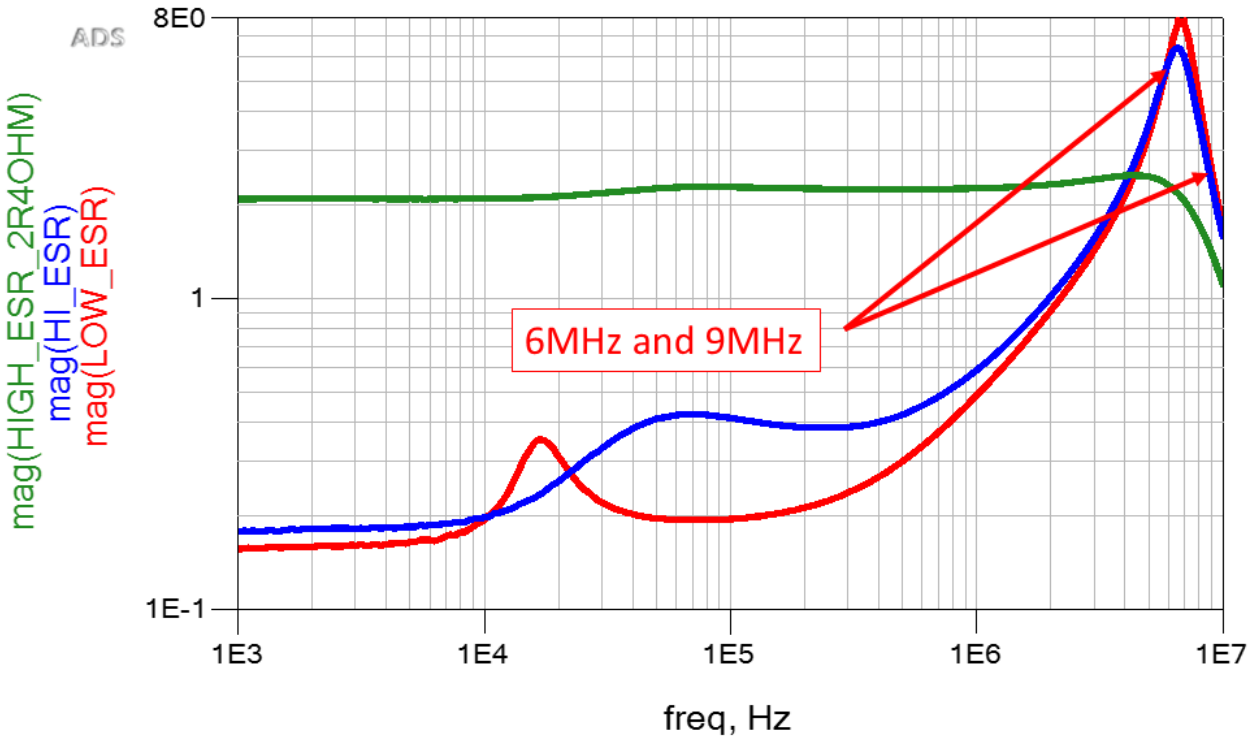


Figure 10: The 7.5MHz resonance (red, blue traces) is clearly seen for two different linear regulator output capacitors, selected with switch S301. The insertion of the 2.4Ω resistor damps the resonance (green trace), reducing the impedance at 7.5MHz by approximately 15dB.

While the sidebands may not have seemed all that severe, they can significantly impact performance; much more so than they might otherwise appear. First, note that the sidebands in Figure 3 appear at 6MHz, while we determined the PCB resonance is at 7.5MHz. Second, the measurement in Figure 10, shows that at 6MHz the impedance is approximately 5dB lower than at the 7.5MHz peak and at 9MHz the impedance is approximately 15dB lower than the 7.5MHz peak.

So, what excited the resonance? There is a 3MHz switching point-of-load (POL) regulator also located on the VRTS3 demo board. The 2nd and 3rd harmonics are close enough to the resonant peak to impart clock noise. We can confirm the POL switching frequency as the noise generator, since an enable switch is included on the VRTS3 training board for this purpose. If we turn off the switching regulator the clock sidebands at 6MHz disappear. This also clearly demonstrates why we want to interrogate the circuit even if it appears to be functional.

The switching regulator operating frequency has a tolerance of 750kHz while the decoupling capacitor also has tolerances. These tolerances can easily shift the second harmonic of the switching regulator to occur exactly at the frequency of the impedance peak, increasing the

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clock noise significantly. While you would not likely see this frequency alignment occur in a nominal test, you are much more likely to know about its possibility via this PDN interrogation.

In summary, we quickly identified a PDN sensitivity that resulted in increased clock jitter. We identified the noise, determined its source and characteristic impedance, and easily corrected the issue by flattening the power rail impedance at the clock. This was all accomplished in just a few minutes using a highly portable harmonic comb generator (Picotest J2150A), a handheld 1-Port probe (Picotest P2100A) and an oscilloscope (Keysight Infiniium S).

Picotest offers several bundled solutions for optimizing, testing, and troubleshooting power integrity issues, such as clock jitter, with support for various instruments and measurement domains. The recently introduced J2150A harmonic comb generator paired with a P2100A 1-port probe is only one, albeit powerful, solution.

ENA Power Integrity Bundles -
https://www.picotest.com/products_Picotest_Keysight_ENA_PNA_Solution.html

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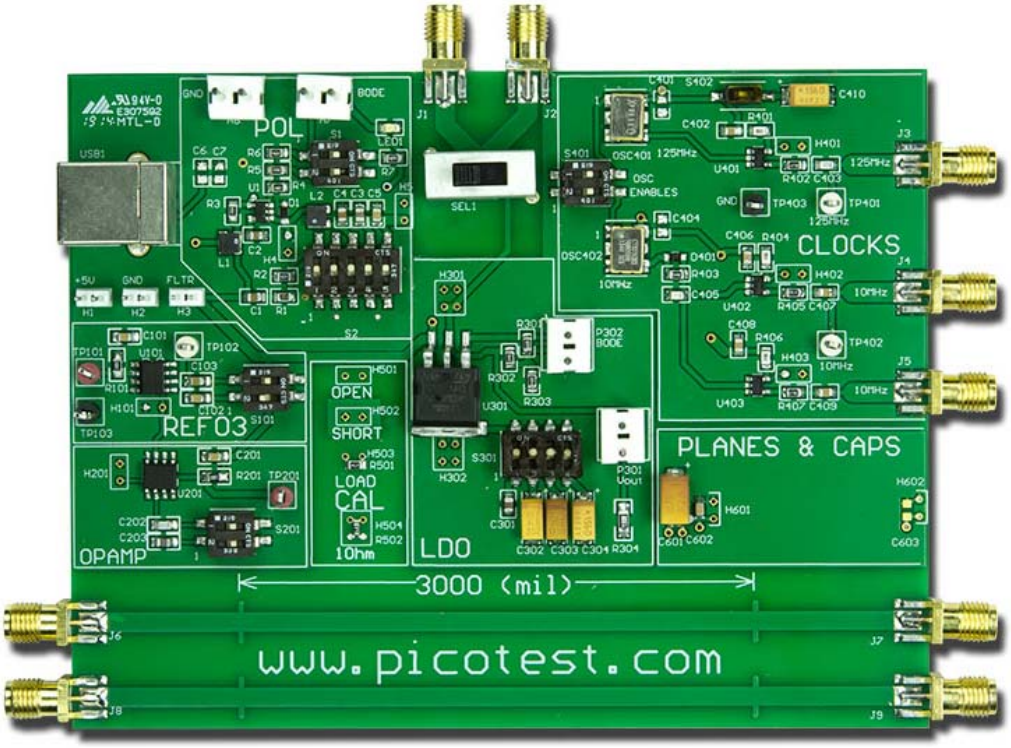
Spectrum Analyzer/RSA Power Integrity Bundles -
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SIDEBAR

Power Integrity Training Test Board

The Picotest VRTS3 demonstration board is an excellent training tool for all levels of test and design engineers. It includes an example for this noise application, as well as many other basic power supply tests including Bode plots, non-invasive stability measurement, PSRR, TDR, and load step.

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