# Debugging I²C Buses in Embedded System Designs

## I²C (Inter Integrated Circuit)

I²C ( sounded I squared C) stands for “Inter Integrated Circuit”. Philips developed it in the early 1980’s to provide a low-cost way of connecting controllers to peripheral chips in TV sets, and became a worldwide standard for communications between devices in embedded systems.

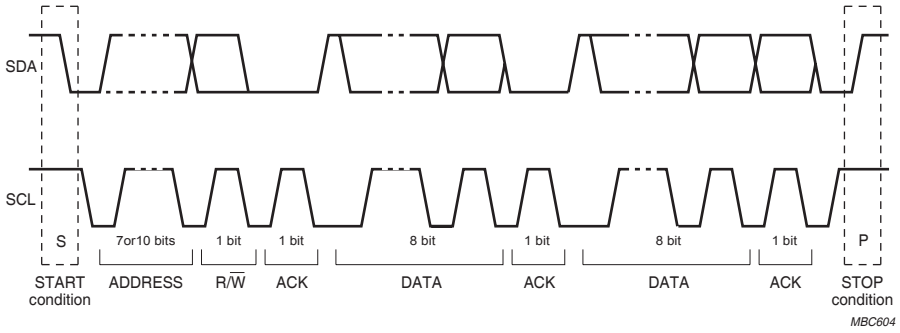
## I²C Applications & Chipmakers

2-wire interface of I²C buses are implemented in wide varied chips like I/O, A/D’s, D/A’s, temperature sensors, microcontrollers and microprocessors from numerous leading chipmakers as Atmel, Analog Devices, Infineon, Intel, Cyprus, Philips, Microchips, ST Microelectronics, Texas Instruments, and others.

## I²C Bus Definition

The 2-wire interface with one master and multiple slaves, and the multi-master configurations are possible.

Signals constructed by DATA(SDA) signal which is always bi-directional, and CLOCK(SCL) signal which is bi-directional only in multi-master mode, and Ground.




A complete data transfer.

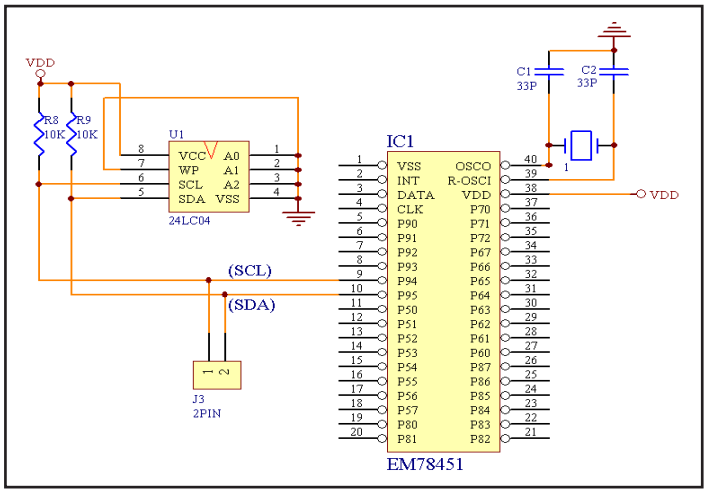
## I²C Bus definition:

**Start:**
SDA signal is going low while SCL signal is high.
**Address:**
a 7 or 10 bit number representing the address of the device that either be read from or written to.
**Read/Write Bit (R/W):**
one bit indicating if the data will be read from or written to the device.
**Acknowledge Bit (ACK):**
one bit from the slave device acknowledging the master’s actions. Usually each address and data byte has an acknowledge bit, but not always.
**Data:**
an integer number of bytes read or written to the device. Data can change while the clock is low. Data should remain stable while the clock signal is going high.
**Stop:**
SDA signal is going high while SCL signal is high.

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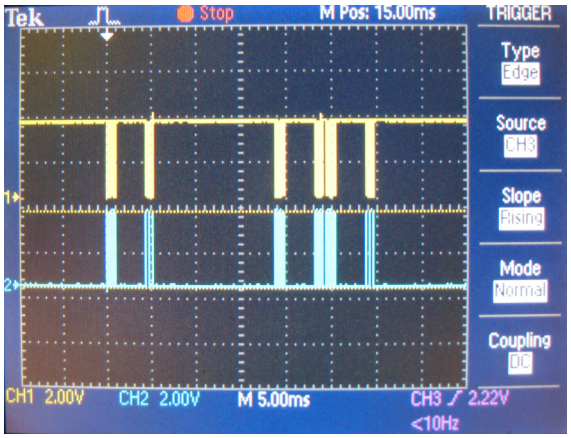
**Debugging I²C Buses**
**By Using Oscilloscope vs. Zeroplus PC based Logic Analyzer**

**Example:**
**Measure an I²C Bus which was written into Microchip EEPROM 24LC02 by ELAN EM78P451 Microcontroller.**
**Master device: ELAN EM78P451**
**Slave device: Microchip EEPROM 24LC02**




## Debugging I²C Bus by Using Oscilloscope

☞ 1st Step:

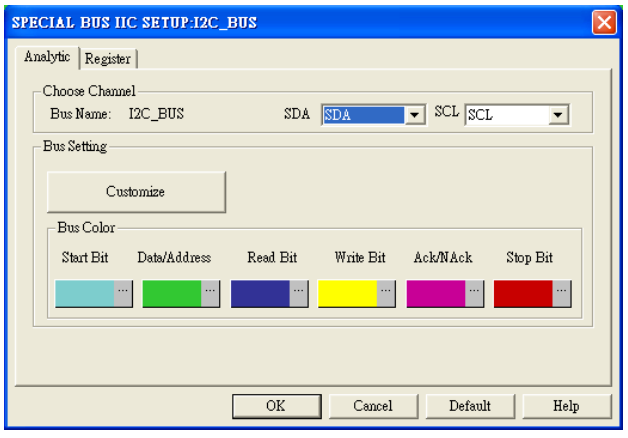



Setup conditions of oscilloscope to catch I²C signal.
Trigger level: CH3 ring edge.
Frequency: <10Hz

Operating time consumed : 10~15 seconds.

## Debugging I²C Bus by Using Zeroplus PC Based Logic Analyzer

☞ 1st Step:



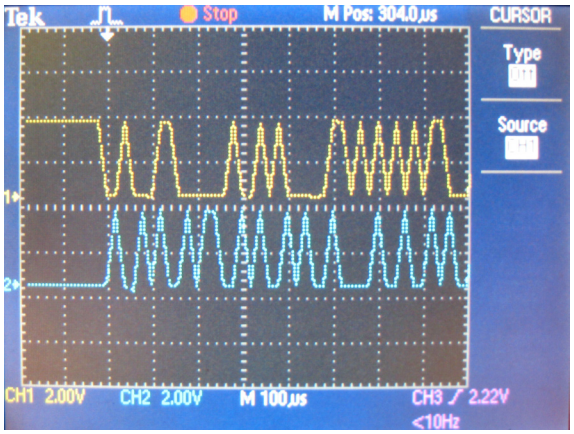

Setup I²C signal conditions on I²C bus analyzer interactive window.

Set trigger condition as below:
SDA: falling edge
SCL: high

Operating time consumed : about 8 seconds.

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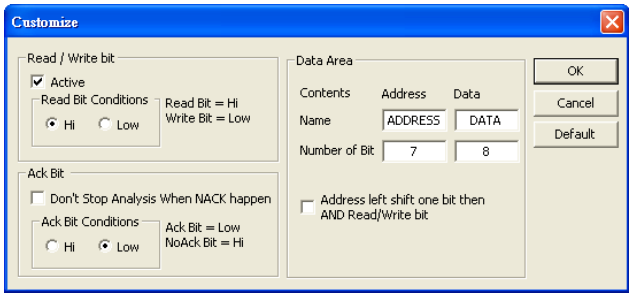
## 2nd Step:




Enlarge screen, and the data can't be recognized.
Setup frequency to re-sampling.

Operating time consumed : about 5 seconds.

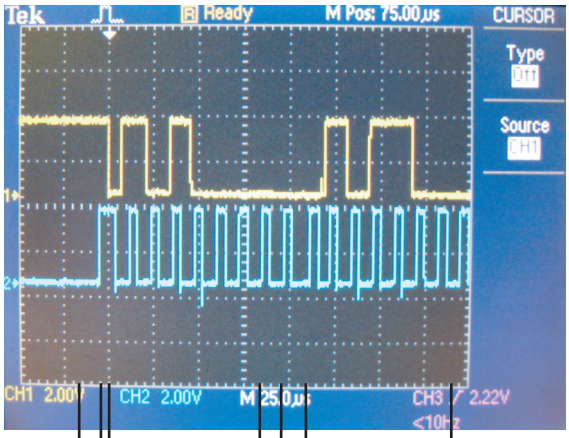
## 2nd Step:




Set up I²C Bus self-definitions.

Operating time consumed : 2~5 seconds.

## 3rd Step:




**I²C signal calculating :**




$2^6\ 2^5\ 2^4\ 2^3\ 2^2\ 2^1\ 2^0$
$1\ \ 0\ \ 1\ \ 0\ \ 0\ \ 0\ \ 0_{(2)}$ $= (2^6x1)+(2^5x0)+(2^4x1)+(2^3x0)+(2^2x0)+(2^1x0)+(2^0x0)$

$= 80_{(10)}$

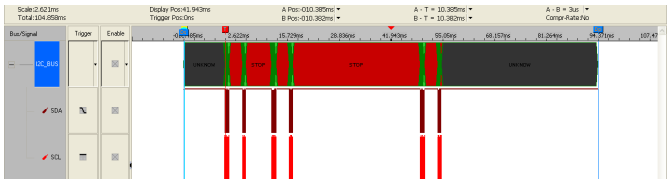
80/16=5.....0

$80_{(10)}=50_{(16)}$

Re-setup oscilloscope at right sampling to catch I²C signal.
Decoding I²C signal manually.

Operating time consumed :
8~10 munutes are consumed to decode an Address & 8 bits data.

## 3rd Step:



Whole I²C signals catch as the figure below:



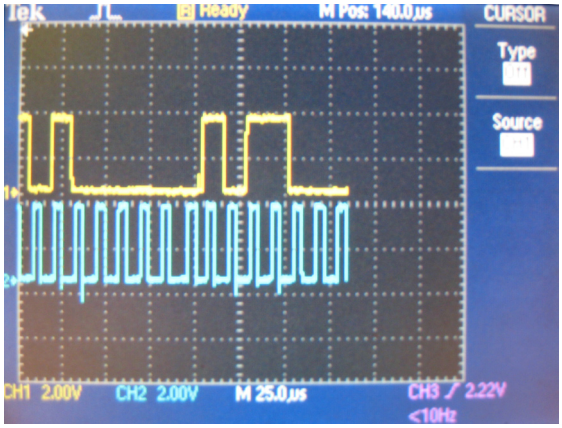
Click " run" icon.

Enlarge I²C signals catch to view and analysis the signals clearly and easily.

Operating time consumed : 20~30 seconds.

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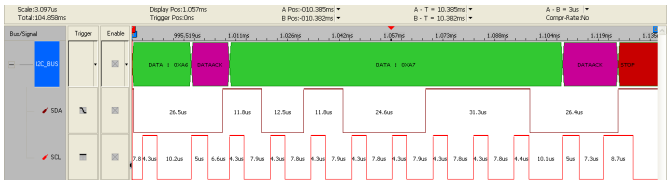
☞ 4th Step:




Only few data of " address bus & data bus " could be captured per right sampling implemented.

Operating time consumed : 5~7 days to decode & debug a project.

☞ 4th Step:



Shift roll bar to view more data depending on LAP-A series model provided.

Operating time consumed : 2~3 days to debug a project.

**Conclusion**

I²C buses are widely implemented in embedded systems design, but the engineers are facing to take extremely time consuming and error prone process to have to manually decoded a long period of bus activity to diagnose problems. Zeroplus PC Based Logic Analyzers provide powerful trigger, decode, and search capabilities for the engineers to solve embedded system design issues with exceptional efficiency.

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