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Logic Analyzer Memory Difference Comparison



~ 64K/128K v.s 2M Memory Depth's Effect on Digital Signal Measurement ~

How to choose Logic Analyzer? Three Demands of one-time Solution

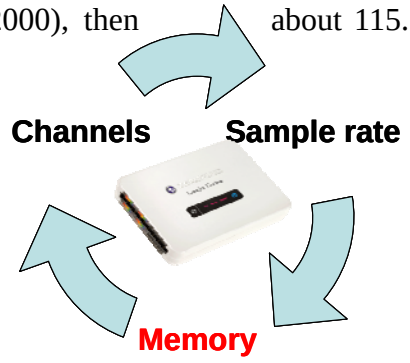
※ What are the "three demands" ?

While purchasing the Logic Analyzer(LA), most users always give priority to "channel quantity", "sampling frequency" and "memory depth", of which especially the sampling frequency and memory depth are the key to analyze digital signal.

The sampling frequency is to separate a period of signal into several points and digitize them, that is, the sampling quantity within one second; the memory depth determines how much logic status data acquired with sampling frequency can be stored. These two factors are important for any digital signal analysis.

For example, if the object under test is I2C 3.4MHz (High Speed-mode), we set the sampling frequency as 18MHz (under the asynchronous condition, the sampling frequency is advised to be four or five times higher than that of the object under test in order to avoid signal distortion.), and set the memory depth as 2M(LAP-C 162000), then about 115.3ms signal can be captured, see below formula:

- Total memory: 2M=2*1024*1024=2,097,152bits
- Sampling frequency: 18MHz = 1/18≒55ns
- Result: 2,097,152bits*55ns≒115.3ms



Pic.1 : 3 demands

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In other words, both sampling frequency and memory depth adjustments will affect the time of signal captured by LA. If we see the sampling frequency as a car's engine, then the memory is the road; the car, though being able to run most quickly, cannot show its capability out if there is no long road for its driving.

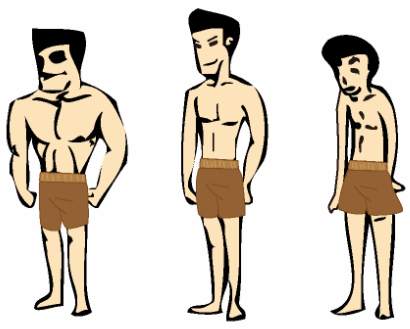
※ Why should they be done once?

It is necessary to have effective tools to do work well. Since we are not able to predict the trend of science and technology, all we can do is to get the tools ready so that we can develop new products fast by keeping pace with progresses and changes of technology. Besides hundreds of protocol analyzers, Zeroplus also provides a variety of logic analyzers of different specifications for users to choose. See below table for the specifications of C series' main products.

<Table 1>: products' specifications comparison table

Product Model	LAP-C 16064	LAP-C 16128	LAP-C 162000
Digital Channel	16	16	16
Internal Clock (Timing Mode)	100 M	200 M	200 M
External Clock (State Mode)	75 M	100 M	100 M
Memory (per channel)	64 k bits	128 k bits	2 M bits
Max. memory for Compression	16 M bits	32 M bits	512 M bits

Seen from the table above, basically, there are just a little bit of differences among these three LAs in hardware efficiency and software function. The biggest difference is the memory depth, seeming that it doesn't actually affect the signal capture, but in fact, this is one of the most important qualities making one LA different from others.



Congenital constitution differences

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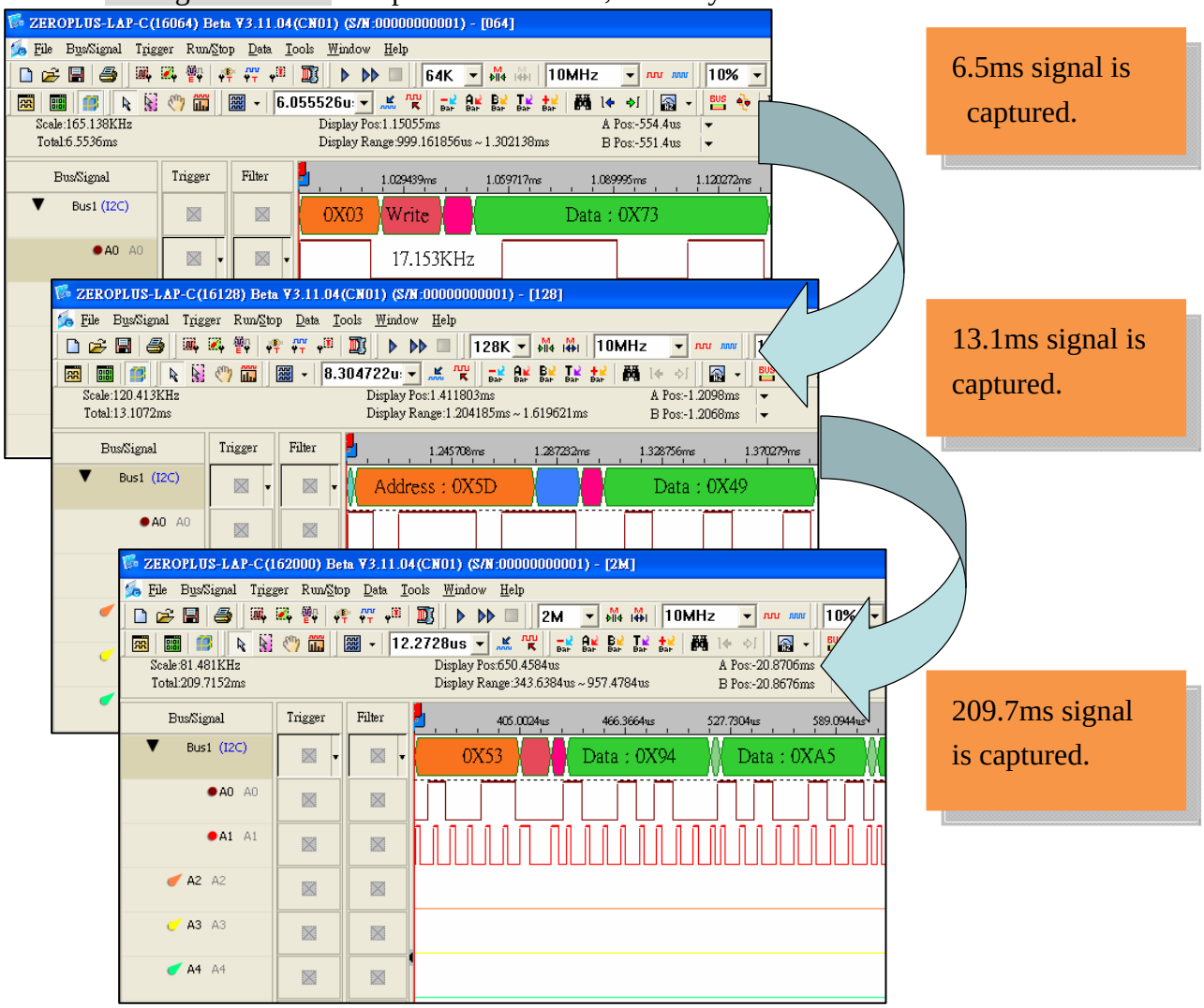
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Difference Reflection of Memory Capacity

※ Capture time

Here we use **LAP-C16064, LAP-C16128 and LAP-C162000** of Zeroplus separately to capture signal from the same object under test (I^2C-Standard speed) and compare their results.

Setting conditions: Sample rate = 10MHz, Memory = 64k / 128k / 2M



6.5ms signal is captured.

13.1ms signal is captured.

209.7ms signal is captured.

Seen from the results above, the larger the memory depth is, the longer signal can be captured. The length of signal captured by 2M memory depth is as much as 32 times higher than that of signal captured by 64K memory depth. We believe such advantage can give better help for the engineers in debugging or analyzing.



High efficiency

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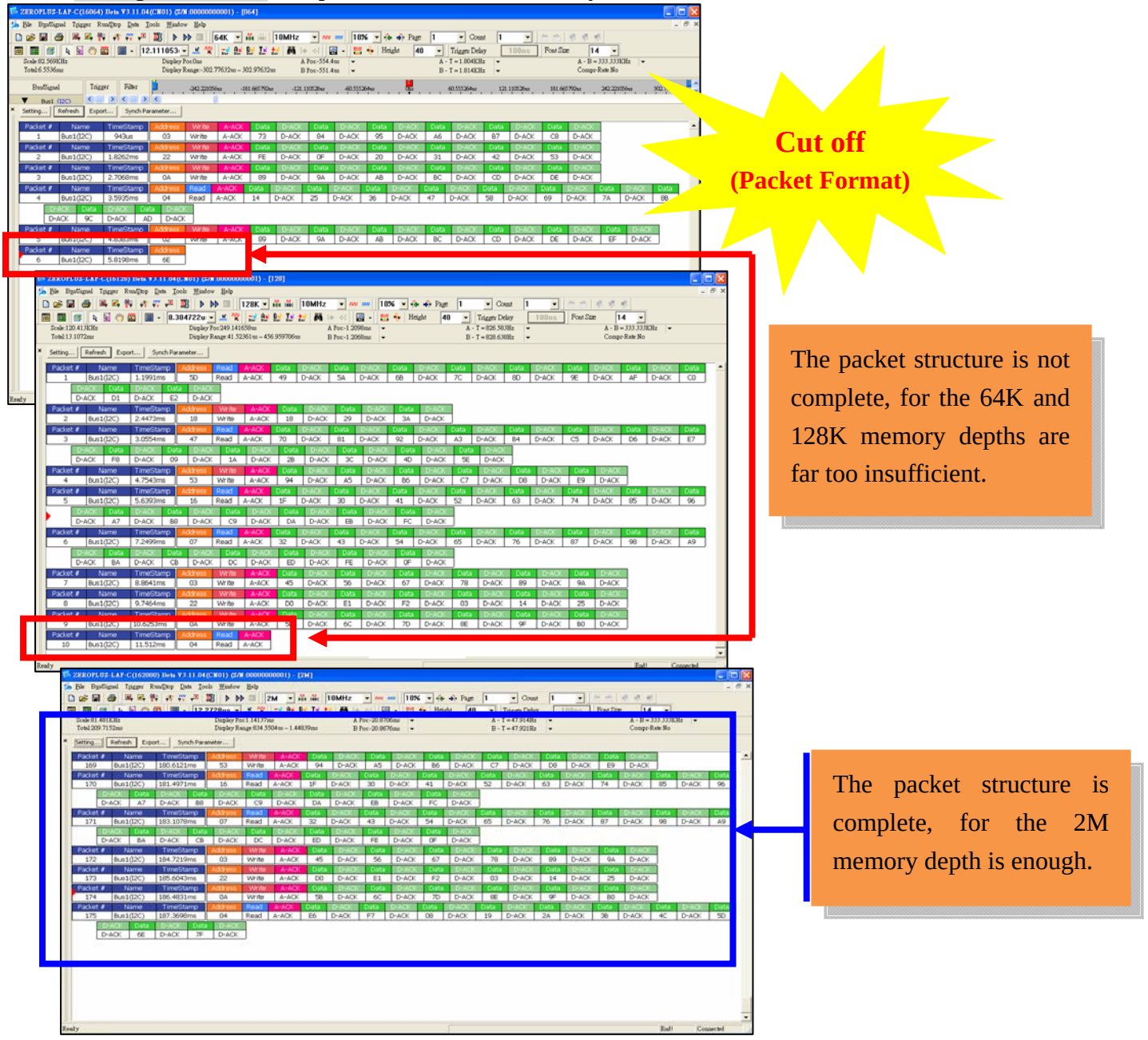
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※ Continuity of Packet Data Protocol

One advantage of high memory is that the continuity of packet data is higher. Engineers always mostly want to see more packets because that will help to analyze the relationship among packets, and this could be achieved by higher memory depth.

Here we also use **LAP-C16064, LAP-C16128 and LAP-C162000** of Zeroplus separately to capture signal from the same object under test (IIC-Standard speed) and compare their results.

Setting conditions: Sample rate = 10MHz, Memory = 64k / 128k / 2M



It is obviously seen from the pictures above that the LA with a higher memory depth can acquire longer signal and more packets, which helps the engineers to do analysis.

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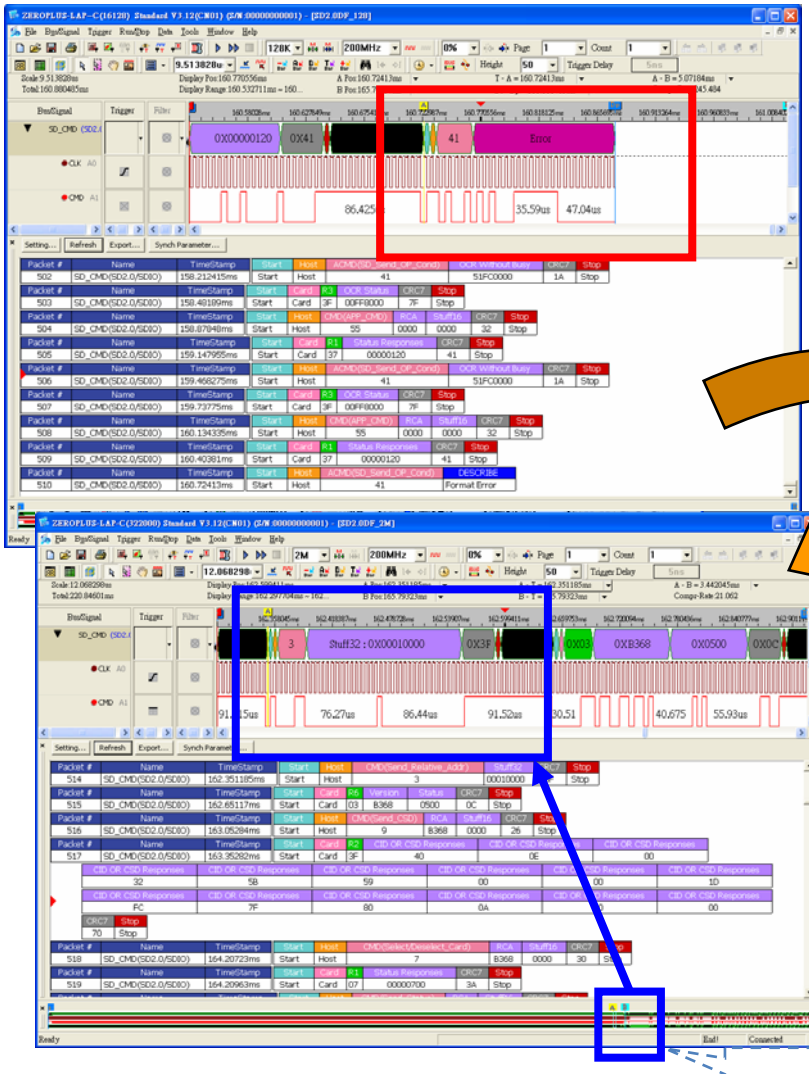
Practice Examples for SD2.0

How long does it take at least to measure a common SD2.0 card? Take the "Initial flow" most frequently analyzed by the engineers for example, see below figure, at least 165.79ms is needed between "Power On" and "Data Transfer Mode". So what differences are there if LAs with 128K and 2M memory are taken respectively to do SD2.0 signal analysis?



Pic.2 : SD2.0 Initial flow

The frequency of SD2.0 is 50MHz, we suggest the LA sample rate setting at 200MHz. See below pictures for the difference between 128K and 2M memory depth.



The LA with 128k memory depth can only capture 160.88ms signal one time during data transmission of SD card, the later data is cut off. (Error!!).

The LA with 2M memory depth can capture 220.84ms signal one time, which is enough for analyzing the action of Initial flow CMD as well as the following 4bit data.

Device identification Mode and **Data Transfer Mode**

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Summary

Insufficient memory depth will cause the captured data to be too little to analyze the needed signal; on the contrary, enough memory depth allows engineers to capture any wanted signal.

The memory depth affects not only the length of captured signal, but also affects the data continuity during data transmission of digital signal.



The logic analyzer products of ZEROPLUS are believed to be a good solution balancing at both price and efficiency.

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